**UE22CS251B - Microprocessor and Computer Architecture # Hrs - 104**

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| **Class #** | | **Chapter Title / Reference Literature** | | **Topics to be Covered** | | **% of portions covered** | | |
| Reference Chapter | | Cumulative |
| **UNIT 1: Introduction to Microprocessor Architecture & ISA** | | | | | | | | |
| 1 | | **1.6,2.3 of T2,**  **A-3 of T1,**  **pg no: 51-55 of T2**  **Chapter 3.1 to 3.5 of T3**  **6.8,5.6 of T2** | | Introduction, ISA Classification - RISC and CISC | | 25% | | 25% |
| 2 | | Processor design trade-offs**,** ARM Processor Architecture, Register set, Introduction to ARM ISA | |
| 3 | | Data Processing Instructions: Addition and Subtraction with sample programming Examples  Introduction to ARMSIM | |
| 4 | | Data Processing Instruction variants | |
| 5 | | Branch Instructions and Addressing Modes | |
| 6 | | Data Transfer instruction | |
| 7 | | Load and Store with programming examples | |
| 8 | | Conditional Execution | |
| 9-10 | | Multiplication Instructions | |
| 11-13 | | Load Multiple and Store Multiple Instructions | |
| **14-15 L1** | | **Lab 1: ARM7TDMI : ISA Programs** | |
| 16 | | Interrupts and Programming Examples | |
| 17 | | 1.1 Interrupts, Context Switching an overview. | |
| 18 | | Functions | |
| 19 | | Parameter passing Techniques | |
| 20 | | Instruction Encoding 1: Data Processing Instruction | |
| 21 | | Instruction Encoding 2: Data Transfer Instruction | |
| 22 | | Instruction Encoding 3: Branch and other Instructions | |
| 23-24 **L2** | | **Lab 2 : ARM7TDMI : ISA Programs** | |
| **UNIT 2: Pipelining & Basics of Cache** | | | | | | | | |
| 25 | | **4.1,4.2 of Text T2**  **Appendix C-1, C-2,**  **Sec 1.1 , 1.4, 1.5 of T1**  **Appendix B.1, B.2, B.3 of T1** | Introduction to Pipelining (3 & 5 Stage) | | 25% | | 50% | |
| 26 | | Performance Analysis | |
| 27 | | Speed up Calculations | |
| 28 | | Introduction to Pipeline hazards | |
| 29 | | Structural Hazards | |
| 30 | | Data Hazards | |
| 31 | | Data Hazards | |
| 32 | | Data Hazards | |
| 33-34  **L3** | | **Lab 3 : ARM7TDMI : ISA Programs** | |
| 35 | | Control Hazard | |
| 36 | | Control Hazard continued.. | |
| 37 | | Introduction to Branch Prediction | |
| 38 | | Branch Prediction 2 | |
| 39 | | Branch Prediction 3 | |
| 40 | | Performance Analysis, Speed up calculations …..etc | |
| 41 | | Performance Analysis, Speed up calculations – continued | |
| 42-43  **L4** | | **Introduction to MPCA mini Project &**  **Batch Formation** | |
| 44 | | Introduction to Memory Subsystem:  Memory Hierarchy & Bottle neck | |  | |  | |
| Introduction to Cache, Locality of reference | |
| 45 | | Cache Design Philosophy  Block Placement, Block Identification, BlockReplacement, | |
| 46 | | Read / Write issues with cache | |
| 47 | | Direct Map Cache Memory | |
| 48 | | Set Associative Cache Memory | |
| 49 | | Fully Associative Cache Memory | |
| 50  **A1** | | **Assignment -1 on Unit -1 & Unit2** | |
| 51 | | Page Replacement Algorithms | |
| 52 | | Read / Write Policy | |
| 53-54  **L5** | | **Lab 4 Programs : Para Cache Simulator** | |
| **Unit 3 : Cache Optimization & I/O Architecture** | | | | | | | | |
| 55 | |  | Performance Analysis | | 25% | | 75% | |
| 56 | | 1st Optimization | |
| 57 | | 1st Optimization &2nd Optimization with examples | |
| 58 | | 3rd Optimization with examples | |
| 59 | | Write Policy | |
| 60 | | Write Policy | |
| 61-62  **L6** | | **Lab 5 Programs : Para Cache Simulator** | |
| 64 | **Appendix B.3 of T1** | | 4th Optimization with examples | |
| 65 | 5th Optimization with examples | |
| 66 | 6th Optimization with examples | |
| 67 | 6th Optimization with examples | |
| 68 | Memory Introduction to flash storage | |
| 69-70  **L7** | **Lab 6: ARM7TDMI : ISA Plugin Programs** | |
| 71 | Connecting Processors, I/O devices. | |
| 72 | Interfacing I/O Devices to the Processor | |
| 73 | DMA Controller | |
| 74 | Memory and Operating System | |
| 75 | Examples | |
| 76-77  **L8** | **Lab 7: ARM7TDMI : ISA Plugin Programs** | |

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| **UNIT-4: Advances in ArchitectureoursHour** | | | | |
| 78 | **Sec 1.9 of T1,**  **Sec 3.1, 4.1** | Introduction to Parallel Computing | 20% | 100% |
| 79 | Parallel Computing: Introductory concepts and terminology-Flynn’s taxonomy |
| 80-81 | Parallel computing memory architectures |
| **82- 83**  **A2** | **Assignment-2** |
| 84 | parallel programming models |
| 85 | parallel examples: matrix multiplication |
| 86 | Hardware Multi threading |
| 87 | PC- Design Issues |
| 88 | Amdahl’s Law, |
| 89 | Gustafson Law, |
| 90 | Multi-Core Architecture |
| 91-92  **L9** | **L8: Project Review-1** |
| 93 | Multi-Core Architecture continued. |
| 94 | Introduction to GPU Computing |
| 95 | GPU-Continued |
| **96 -97**  **L10** | **L9: Project Work using sensors** |
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| 98-104  **L11** |  | Project Presentation and Demonstration |  |  |
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**Literature:**

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| --- | --- | --- | --- | --- | --- |
| Book Type | Code | Title & Author | Publication Info | | |
| Edition | Publisher | Year |
| Text Book | T1 | “Computer Organization and Design “, Hennessy Patterson | Fifth Edition | MK Morgan Kaufmann | 2012 |
| Text Book | T2 | “ARM System-on-Chip Architecture”, Steve Furber | Second Edition, | Pearson Education | 2000 |
| Text Book | T3 | Computer Organization and Design – ARM Edition | Reprint 2009 | Elsevier | 2009 |